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PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Eric R. Fossum et al. Art Unit: 2612
Serial No.: 09/749,989 Examiner: Unknown
Filed : December 26, 2000
Title : AN ACTIVE PIXEL SENSOR PIXEL HAVING A PHOTODETECTOR WHOSE OUTPUT IS COUPLED TO AN OUTPUT TRANSISTOR GATE (**Amended**)

Commissioner of Patents and Trademarks
Washington, DC 20231

RESPONSE TO NOTICE OF OMITTED ITEM(S) AND PRELIMINARY AMENDMENT

Sir:

In response to the Notice of Omitted Item(s) mailed January 30, 2001 (copy enclosed), please amend the application as follows:

In the Specification:

On page 11, delete lines 13-14.

On page 34, line 5, delete -- FIG. 10 shows --.

Additionally, prior to formal examination of the above-referenced application, kindly enter the following amendments:

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

February 16, 2001
Date of Deposit

Nancy Grant
Signature

Nancy Grant
Typed or Printed Name of Person Signing Certificate

In the Title:

Please amend the title to read as follows:

--AN ACTIVE PIXEL SENSOR PIXEL HAVING A PHOTODETECTOR WHOSE OUTPUT IS COUPLED TO AN OUTPUT TRANSISTOR GATE--.

In the Specification:

Page 27, line 8, delete "can be extended".

Page 28, line 14, delete "via capacitor 1004".

Page 34, line 5, replace "a graph of β the ratio" with --The saturation level N_{sat} increases as the ratio β--.

Page 34, lines 7-8, delete "as β increases, the saturation level N_{sat} increases as".

In the Claims:

Please amend claim 1 as follows:

1. **(Amended)** An imaging device, comprising:

a monolithic semiconductor integrated circuit substrate;

a focal plane array of pixel cells, each one of said pixel cells comprising: [,]

a photodetector having a photodetector portion formed in said substrate and a photodetector electrode overlying said

photodetector portion, said photodetector operable to accumulate photo-generated charge in said photodetector portion in response to incident radiation, and

[a photogate overlying said substrate capable of accumulating photo-generated charge in an underlying portion of said substrated, and]

a charge coupled device section formed on said substrate adjacent said [photogate] **photodetector and having an output transistor whose gate is connected to said photodetector electrode to form a floating gate and at least one charge coupled device stage, said charge coupled device section configured and operable to transfer charge through said charge coupled device stage from said photodetector portion of said substrate to a drain of said output transistor during a reset operation and to produce an electrical signal indicative of said photo-generated charge** [a sensing node and at least one charge coupled device stage capable of transeferring charge from said underlying portion of the substrate to said sensing node].

Please add the following new claims:

2. **(New)** The imaging device of Claim 1 wherein said charge coupled device stage comprises a transfer gate between

said drain of said output transistor and said photodetector portion.

3. **(New)** The imaging device of Claim 2, wherein said charge coupled device section includes a capacitor having a first terminal coupled to both said floating gate of said output transistor and said photodetector electrode and a second terminal to receive a row address voltage signal that is at an integration voltage higher than a barrier potential at said transfer gate during an integration period and is at a readout voltage which is higher than said integration voltage during a readout period.

4. **(New)** The imaging device of Claim 1 further comprising means for periodically resetting a potential of said floating gate to a predetermined potential.

5. **(New)** The imaging device of Claim 1, wherein each one of said pixel cells further comprises:

a drain diffusion connected to a drain bias voltage; and

a reset gate located between said floating gate of said output transistor and said drain diffusion and coupled to receive a reset control signal that controls said reset operation.

6. **(New)** The imaging device of Claim 1, further comprising a readout circuit which includes a field effect source follower output transistor having a gate coupled to receive an output from said floating gate of said output transistor.

7. **(New)** The imaging device of Claim 6, wherein said readout circuit further comprises a field effect load transistor connected to said source follower output transistor.

8. **(New)** The imaging device of Claim 7, wherein said readout circuit further comprises a correlated double sampling circuit having an input node connected between said source follower output transistor and said load transistor.

9. **(New)** The imaging device of Claim 8, wherein the correlated double sampling circuit comprises:

a pair of sample and hold field effect transistors formed in said substrate, each sample and hold field effect transistor having one of a source and drain thereof connected to a source of said source follower transistor;

a pair of sample and hold capacitors connected to the other one of the source and drain of a respective one of said pair of sample and hold transistors; and

means for sensing a potential of each of said sample and hold capacitors at respective intervals.

10. **(New)** The imaging device of Claim 9 further comprising means for sensing a difference between potentials of said pair of sample and hold capacitors.

11. **(New)** The imaging device of Claim 9 further comprising means for shorting across each of said pair of sample and hold capacitors simultaneously while said means for sensing measures a fixed pattern noise difference.

12. **(New)** The imaging device of Claim 9, wherein said focal array of pixel cells is organized in rows and columns, and wherein said readout circuit further comprises a plurality of load transistors and correlated double sampling circuits, wherein each cell in each column of pixel cells is connected to a single common load transistor and a single common correlated double sampling circuit.

13. **(New)** The imaging device of Claim 12, wherein each of said common load transistors and correlated double sampling circuits is disposed at an end of a respective column of pixel cells connected thereto.

14. **(New)** The imaging device of Claim 12, wherein said readout circuit further comprises:

a row select field effect transistor formed in each one of said cells having its source and drain connected between said source of said source follower output transistor and said pair of sample and hold transistors, and a gate connected to a row select signal; and

wherein said means for sensing at period intervals comprises,

a pair of sample and hold output transistors having respective gates and sources connected across respective ones of said pair of sample and hold capacitors, and having respective drains,

respective differential output nodes of said correlated double sampling circuit, and

a pair of column select transistors formed in said substrate each having a source and drain connected between a drain of a respective one of said sample and hold output transistors and a gate connected to a column select signal.

15. **(New)** The imaging device of Claim 14, wherein each of said transistors is a metal oxide field effect transistor, said source follower output transistor, said load transistor,

said row select transistor, and said pair of sample and hold transistors being n-channel devices, said pair of sample and hold output transistors and said pair of column select transistors being p-channel devices.

16. **(New)** The imaging device of Claim 1 further comprising a micro-lens layer overlying said substrate, said micro-lens layer comprising:

a refractive layer; and

individual lenses formed in said layer in registration with individual ones of said cells, each of said individual lenses having a curvature for focusing light toward a photosensitive portion of the respective cell.

17. **(New)** The imaging device of Claim 16, wherein said refractive layer comprises a polymer.

18. **(New)** The imaging device of Claim 17 wherein said refractive layer comprises polyamide.

19. **(New)** The imaging device of Claim 16, wherein each of said individual lenses covers portions of the corresponding cell including said photodetector as well as said charge coupled device section.

20. **(New)** The imaging device of Claim 1, further comprising CMOS image signal processing electronics integrated on said substrate and connected to communicate with said focal plane array, said CMOS image signal processing electronics providing on-chip signal processing of electrical signals from said pixel cells.

21. **(New)** An imaging device, comprising:

a monolithic semiconductor integrated circuit substrate;

a focal plane array of pixel cells formed on said substrate by an integrated circuit process that is compatible with a complementary metal oxide semiconductor (CMOS) process, each one of said pixel cells comprising:

a photodetector electrode overlying said substrate and operable to accumulate photo-generated charge in an underlying photodetector portion of said substrate,

a barrier gate formed on said substrate adjacent said photodetector portion, and

a pixel transistor formed on said substrate and configured to have a first diffusion region adjacent said barrier gate, a gate and a second diffusion region, said gate connected to said photodetector electrode to form a floating gate,

wherein said barrier gate is operable to transfer said photo-generated charge from said underlying photodetector portion of said substrate to said first diffusion region of said pixel transistor, and wherein said gate of said pixel transistor produces an electrical signal comprising a signal component indicative of said photo-generated charge and a noise component indicative of noise associated with said pixel; and

MOS image signal processing electronics integrated on said substrate and connected to communicate with said focal plane array and to provide on-chip signal processing of electrical signals from said pixel cells.

22. **(New)** The imaging device of Claim 21, wherein said first diffusion region is a floating node to function as a source of said pixel transistor and said second diffusion region is biased at a selected DC voltage to function as a drain, said first diffusion region converting said photo-generated charge into said electrical signal.

23. **(New)** The imaging device of Claim 22, further comprising:

a readout circuit formed on said substrate and comprising a field-effect source follower output transistor coupled to receive said electrical signal from said pixel transistor;

a field-effect load transistor connected to said source follower output transistor; and

a correlated double sampling circuit having an input node connected between said source follower output transistor and said load transistor and operable to produce an output signal indicating only said photo-generated charge, wherein said sampling circuit samples said electrical signal once when said gate of said pixel transistor is set at a first gate potential without changing an amount of photo-generated charge in said first diffusion region and to sample said electrical signal for a second time when said gate of said pixel transistor is set at a second gate potential.

24. **(New)** The imaging device of Claim 21, wherein said first diffusion region is biased at a selected DC voltage to function as a drain.

25. **(New)** The imaging device of Claim 24, wherein each pixel cell further comprises a capacitor having a first terminal connected to both said photodetector electrode and said gate of said pixel transistor.

26. **(New)** The imaging device of Claim 24, further comprising:

a readout circuit comprising a field-effect source follower output transistor formed in each one of said cells, the second diffusion region of said pixel transistor being connected to a gate of said source follower output transistor;

a field-effect load transistor connected to said source follower output transistor; and

a correlated double sampling circuit having an input node connected between said source follower output transistor and said load transistor and operable to sample said second diffusion region twice in an readout operation to produce an output signal indicating only said photo-generated charge.

27. **(New)** An imaging device, comprising:

a monolithic semiconductor integrated circuit substrate;

a focal plane array of pixel cells formed on said substrate by an integrated circuit process that is compatible with complementary metal oxide semiconductor (CMOS) process, each one of said pixel cells comprising,

a photodetector electrode overlying said substrate and operable to accumulate photo-generated charge in an underlying portion of said substrate,

a barrier gate formed on said substrate adjacent said underlying portion, and

a pixel transistor formed on said substrate and configured to have a drain adjacent said barrier gate, a gate and a source,

a capacitor having a terminal connected to both said photodetector electrode and said gate of said pixel transistor to make said gate of said pixel transistor a floating gate,

wherein said barrier gate is operable to transfer said photo-generated charge from said underlying portion of said substrate under said photodetector electrode to said drain of said pixel transistor which produces an electrical signal having a signal component indicative of said photo-generated charge.

28. **(New)** The imaging device of Claim 27, further comprising a readout circuit formed on said substrate to receive said electrical signal, said read circuit comprising:

a field-effect source follower output transistor coupled to receive said electrical signal;

a field-effect load transistor connected to said source follower output transistor; and

a correlated double sampling circuit having an input node connected between said source follower output transistor and said load transistor and operable to sample said second diffusion region twice in a readout operation to produce an output signal indicating only said photo-generated charge.

29. **(New)** The imaging device of Claim 27, further comprising CMOS image signal processing electronics integrated on said substrate and connected to communicate with said focal plane array, said CMOS image signal processing electronics providing on-chip signal processing of electrical signals from said pixel cells.

30. **(New)** A method, comprising:

producing charge in a portion of a semiconductor substrate under a photodetector electrode in response to incident photons incident to said portion;

using a transfer gate formed in said substrate next to said portion under said photodetector electrode to output said charge;

using a drain of an output transistor formed in said substrate next to said transfer gate to receive said charge from said portion; and

connecting a gate of said output transistor to said photodetector electrode to form a floating gate so as to convert said charge into an electrical signal.

31. **(New)** A method as in claim 30, further comprising biasing said drain at a DC voltage.

32. **(New)** A method as in claim 30, further comprising:

coupling a first terminal of a capacitor to both said photodetector electrode and said gate of said output transistor;

using a second terminal of said capacitor to receive a row address voltage; and

using a source of said output transistor to receive a row address voltage.

33. **(New)** A method as in claim 32, further comprising:

setting said row address voltage at an integration voltage higher than a barrier potential at said transfer gate during an integration period; and

setting said row address voltage at a readout voltage which is higher than said integration voltage during a readout period.

REMARKS

All reference to Figure 10 has been removed from the Specification to obviate the Notice of Omitted Item(s).

In addition, the following amendment is made herein. Claim 1 is amended and new Claims 2-33 are added. Furthermore, the specification is amended to correct certain typographical errors. The amendment is fully supported by the specification as originally filed. No new matter is added. Hence, upon entry of the above amendment, Claims 1-33 are now pending.

Applicants respectfully submit that Claims 1-33 are patentable and request a formal notice to that effect.

Please charge any deficiencies or credit any overpayment to our Deposit Account No. 06-1050.

Respectfully submitted,

Date: 2-16-01

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